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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,891	07/30/2003	Thomas R. Woodall	PD-02W207	7948

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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,891	WOODALL, THOMAS R.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/30/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-28 are pending.

2. The office acknowledges the following papers:

Patent Application filed on 7/30/2003.

Priority

3. The effective filing date for the subject matter defined in the pending claims in this application is 1/17/2002.

Drawings

4. The Examiner contends that the drawings submitted on 7/30/2003 are acceptable for examination proceedings.

Specification

5. The disclosure is objected to because of the following informalities:

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The Applicant's cooperation is requested in correcting any errors of which the Applicant may become aware.

7. Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 12-28 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 12 and 21 recite the limitation "a second plurality of functional units for comparing internal streams with a debug stream to generate debug signals." The term internal streams is unclear because the specification doesn't define what an internal stream is that is being compared to the debug stream.

10. Claims 13-20 and 22-28 are rejected due to their dependency.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1, 4-9, 12, 15-21, and 24-28 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bates et al. (U.S. 7,080,360).

13. As per claim 1:

Bates disclosed a stream computer, said stream computer comprising:

A plurality of interconnected functional units, each of said functional units responsive to a data stream containing data to be operated on by one or more of said functional units (Bates: Figure 4, column 6 lines 57-67)(Figure 4 shows the program

code that is executed on the processor. It would have been obvious to one of ordinary skill in the art at the time of the invention that the code when assembled would include compare, addition, load, and branching instructions. It would have been obvious to one of ordinary skill in the art at the time of the invention that these instructions would be performed on multiple functional units, instead of a single functional unit.);

Digital logic cooperatively associated with one of said functional units for comparing said data stream presented to said one of said functional units with a debug stream (Bates: Figure 5 elements 508, 520, and 528, column 8 lines 1-13 and column 10 lines 17-41)(For conditional breakpoints, a value is being compared from the data stream to the debug stream to see if a conditional breakpoint has occurred.);

Reporting logic associated with said digital logic for reporting the occurrence of matches between said data stream and said debug stream (Bates: Figure 5 element 542, column 10 lines 17-41)(When a conditional breakpoint occurs, the information is send to the display.).

14. As per claim 4:

Bates disclosed a stream computer as described in claim 1 wherein said digital logic extracts similarities between said data stream and said debug stream to induce a breakpoint (Bates: Figure 5 elements 516 and 528, column 5 lines 39-55 and column 10 lines 17-41)(A conditional breakpoint compares a value to the data stream to determine if a breakpoint occurred or not.).

15. As per claim 5:

Bates disclosed a stream computer as described in claim 4 wherein said digital

logic extracts similarities between said data stream and said debug stream to induce said breakpoint in response to a breakpoint number arriving at said digital logic (Bates: Figure 5 elements 516 and 528, column 10 lines 1-3 and lines 17-41)(It's obvious to one of ordinary skill in the art that multiple breakpoints could be set when debugging and each breakpoint would have a tag that tells which is which.).

16. As per claim 6:

Bates disclosed a stream computer as described in claim 4 wherein said digital logic generates said breakpoint and interrupts said data stream passing through said digital logic (Bates: Figure 5 elements 516 and 528, column 10 lines 1-3).

17. As per claim 7:

Bates disclosed a stream computer as described in claim 4 wherein said digital logic generates said breakpoint and allows said data stream to pass through (Bates: Figure 5 element 530, column 10 lines 17-41)(If the condition for the breakpoint is false, then the data is allowed to pass through without the breakpoint interrupting the processor.).

18. As per claim 8:

Bates disclosed a stream computer as described in claim 1 wherein said at least one of said plurality of interconnected functional units, said digital logic, and said reporting logic are integrated on a single substrate (Official notice is given that all of the functional units, digital logic, and reporting logic could be on a single chip.).

19. As per claim 9:

Bates disclosed a stream computer as described in claim 1 wherein said

reporting logic are compatible with a graphical user interface, said graphical user interface identifying said functional units, and inputs and outputs of said functional units (Bates: Column 10 lines 17-41)(The breakpoint data is sent to the GUI.).

20. As per claim 12:

Claim 12 essentially recites the same limitations of claim 1. Claim 12 additionally recites the following limitations:

A second plurality of interconnected functional units for comparing internal streams with debug streams (Bates: Figures 5 and 6 element 512, column 6 lines 20-30 and column 8 lines 1 continued to column 10 line 16.)(The safety net breakpoints are also considered internal breakpoints.).

21. As per claim 15:

Claim 15 essentially recites the same limitations of claim 4. Therefore, claim 15 is rejected for the same reasons as claim 4.

22. As per claim 16:

Claim 16 essentially recites the same limitations of claim 5. Therefore, claim 16 is rejected for the same reasons as claim 5.

23. As per claim 17:

Claim 17 essentially recites the same limitations of claim 6. Therefore, claim 17 is rejected for the same reasons as claim 6.

24. As per claim 18:

Claim 18 essentially recites the same limitations of claim 7. Therefore, claim 18 is rejected for the same reasons as claim 7.

25. As per claim 19:

Claim 19 essentially recites the same limitations of claim 8. Therefore, claim 19 is rejected for the same reasons as claim 8.

26. As per claim 20:

Claim 20 essentially recites the same limitations of claim 9. Therefore, claim 20 is rejected for the same reasons as claim 9.

27. As per claim 21:

Claim 21 essentially recites the same limitations of claim 12. Therefore, claim 21 is rejected for the same reasons as claim 12.

28. As per claim 24:

Claim 24 essentially recites the same limitations of claim 4. Therefore, claim 24 is rejected for the same reasons as claim 4.

29. As per claim 25:

Claim 25 essentially recites the same limitations of claim 5. Therefore, claim 25 is rejected for the same reasons as claim 5.

30. As per claim 26:

Claim 26 essentially recites the same limitations of claim 6. Therefore, claim 26 is rejected for the same reasons as claim 6.

31. As per claim 27:

Claim 27 essentially recites the same limitations of claim 7. Therefore, claim 27 is rejected for the same reasons as claim 7.

32. As per claim 28:

Claim 28 essentially recites the same limitations of claim 9. Therefore, claim 28 is rejected for the same reasons as claim 9.

33. Claims 2-3, 13-14, and 22-23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bates et al. (U.S. 7,080,360), further in view of Pardo et al. (U.S. 5,754,839).

34. As per claim 2:

Bates disclosed a stream computer as described in claim 1.

Bates failed to teach wherein said digital logic extracts similarities between said data stream and said debug stream to generate a viewpoint.

However, Pardo disclosed wherein said digital logic extracts similarities between said data stream and said debug stream to generate a viewpoint (Pardo: Figure 2, column 2 lines 30-40)(Watchpoints allow for extracting data without interrupting the processor, which is the same as viewpoints.).

Bates disclosed that the processor allows for watchpoints to occur during the normal debugging process, but failed to teach how this would occur and how a watchpoint functions compared to a breakpoint (Bates: Column 5 lines 8-20). One of ordinary skill in the art would have thus been motivated to learn how a watchpoint functions compared to a breakpoint to make the combination of Pardo and Bates. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the process of handling watchpoints from Pardo for the processor of Bates.

35. As per claim 3:

Bates and Pardo disclosed a stream computer as described in claim 2 wherein said digital logic generates said viewpoint without interrupting said data stream (Pardo: Column 1 lines 41-53).

36. As per claim 13:

Claim 13 essentially recites the same limitations of claim 2. Therefore, claim 13 is rejected for the same reasons as claim 2.

37. As per claim 14:

Claim 14 essentially recites the same limitations of claim 3. Therefore, claim 14 is rejected for the same reasons as claim 3.

38. As per claim 22:

Claim 22 essentially recites the same limitations of claim 2. Therefore, claim 22 is rejected for the same reasons as claim 2.

39. As per claim 23:

Claim 23 essentially recites the same limitations of claim 3. Therefore, claim 23 is rejected for the same reasons as claim 3.

40. Claims 10-11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bates et al. (U.S. 7,080,360), further in view of Master et al. (U.S. 6,836,839).

41. As per claim 10:

Bates disclosed a stream computer as described in claim 1.

Bates failed to teach wherein one or more of said functional units are

reconfigured to become part of said digital logic.

However, Master disclosed wherein one or more of said functional units are reconfigured to become part of said digital logic (Master: Figure 1, column 4 lines 50-64)(The combination of Master and Bates allows for the functional units being developed on a FPGA and thus has the capability of being reconfigured for other uses.).

The advantage of using a FPGA on the ACE system of Master for processing units is that they are reconfigurable after post fabrication, reconfigurable in real time, allow for multiple modes of operation, and minimizes power consumption while increasing performance (Master: Column 3 lines 19-52). These advantages would have motivated one of ordinary skill in the art at the time of the invention to implement a FPGA for use on the processor of Bates. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a FPGA for the processing units of Bates for the above advantages.

42. As per claim 11:

Bates disclosed a stream computer as described in claim 1.

Bates failed to teach wherein said digital logic further comprises arithmetic logic units (ALU) and memory functions, said functions obtained by allocating some functional units to perform said ALU and memory functions.

However, Master disclosed wherein said digital logic further comprises arithmetic logic units (ALU) and memory functions, said functions obtained by allocating some functional units to perform said ALU and memory functions (Master: Figure 1 elements

150c-n, column 5 lines 30-43 and column 7 line 35 continued to column 8 line 19)(The reconfigurable processing units allow for performing memory and ALU functions.).

The advantage of using a FPGA on the ACE system of Master for processing units is that they are reconfigurable after post fabrication, reconfigurable in real time, allow for multiple modes of operation, and minimizes power consumption while increasing performance (Master: Column 3 lines 19-52). These advantages would have motivated one of ordinary skill in the art at the time of the invention to implement a FPGA for use on the processor of Bates. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a FPGA for the processing units of Bates for the above advantages.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ramanadin et al. (U.S. 6,349,371), taught the process of allowing watchpoints during debugging.

Bates et al. (U.S. 6,634,020), taught setting breakpoints and watchpoints for debugging.

Fukushiro et al. (U.S. 5,850,510), taught setting breakpoints and watchpoints for debugging.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
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